L Number	Hits	Search Text	DB	Time stamp
1	224177	softwar	USPAT; US-PGPUB; EP ; JPO; DERWENT; IBM TDB	2002/01/10 19:48
2	204630	hardware	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:48
3	249	DLAT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:48
4	2787	TLB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:48
5	777140	target address	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:48
6	397761	host instruction	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:48
7	24325	emulat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:51
8	86440	software and hardware	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:51
9	51	(software and hardware) and DLAT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:51
10	14	((s ftware and hardware) and DLAT) and TLB	USPAT; US-PGPUB; EP ; JP ; DERWENT; IBM TDB	2002/01/10 19:52

11	14	(((s ftware and hardware) and DLAT) and TLB) and (target address)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:52
12	12	((((software and hardware) and DLAT) and TLB) and (target address)) and (host instruction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:52
13	3	(((((software and hardware) and DLAT) and TLB) and (target address)) and (host instruction)) and emulat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/01/10 19:52

```
=> d his

     (FILE 'HOME' ENTERED AT 19:38:52 ON 10 JAN 2002)

     FILE 'USPATFULL' ENTERED AT 19:40:01 ON 10 JAN 2002
L1            45 S TLB#/TI
L2            54 S HOST INSTRUCTION
L3           140 S DLAT
L4          2485 S TARGET ADDRESS
L5         15858 S EMULAT?

=> s l1 and l3

L6             1 L1 AND L3

=> s l1 and l4

L7             5 L1 AND L4

=> dis 1- pn,ti

YOU HAVE REQUESTED DATA FROM 5 ANSWERS - CONTINUE? Y/(N):y


L7   ANSWER 1 OF 5  USPATFULL
PI     US 6266752          B1   20010724
TI     Reverse TLB for providing branch target
     address in a microprocessor having a physically-tagged cache

L7   ANSWER 2 OF 5  USPATFULL
PI     US 6208543          B1   20010327
TI     Translation lookaside buffer (TLB) including fast hit signal
       generation circuitry

L7   ANSWER 3 OF 5  USPATFULL
PI     US 6079003               20000620
TI     Reverse TLB for providing branch target
     address in a microprocessor having a physically-tagged cache

L7   ANSWER 4 OF 5  USPATFULL
PI     US 5930832               19990727
TI     Apparatus to guarantee TLB inclusion for store operations

L7   ANSWER 5 OF 5  USPATFULL
PI     US 5805490               19980908
TI     Associative memory circuit and TLB circuit
```